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MS-7377(BELEM) uE



CPU: LGA 775 Yorkfiled Qual core --95W
 Wolfdale 1333 , 1066 , 800 -- 45W
 Core 2 duo 1333 E6*50 -- 65W
 Core 2 duo 1066 E6*00 -- 65W
 Core 2 duo 800 E4XXX -- 65W
 Daul Core E2XX --65W
 Celeron 4XX -- 35W

System Chipset:

Intel Bearlake - Q35 (North Bridge)
 Intel ICH9 DO(South Bridge)

On Board Device:

CLOCK Gen -- ICS9LP505-2HLFT 54PIN or Silego 84516BT
 LPC Super I/O -- ITE8718
 LAN-- Intel 82566MM
 HD Audio Codec -- ALC888

Main Memory:

Dual-channel DDR-II * 4

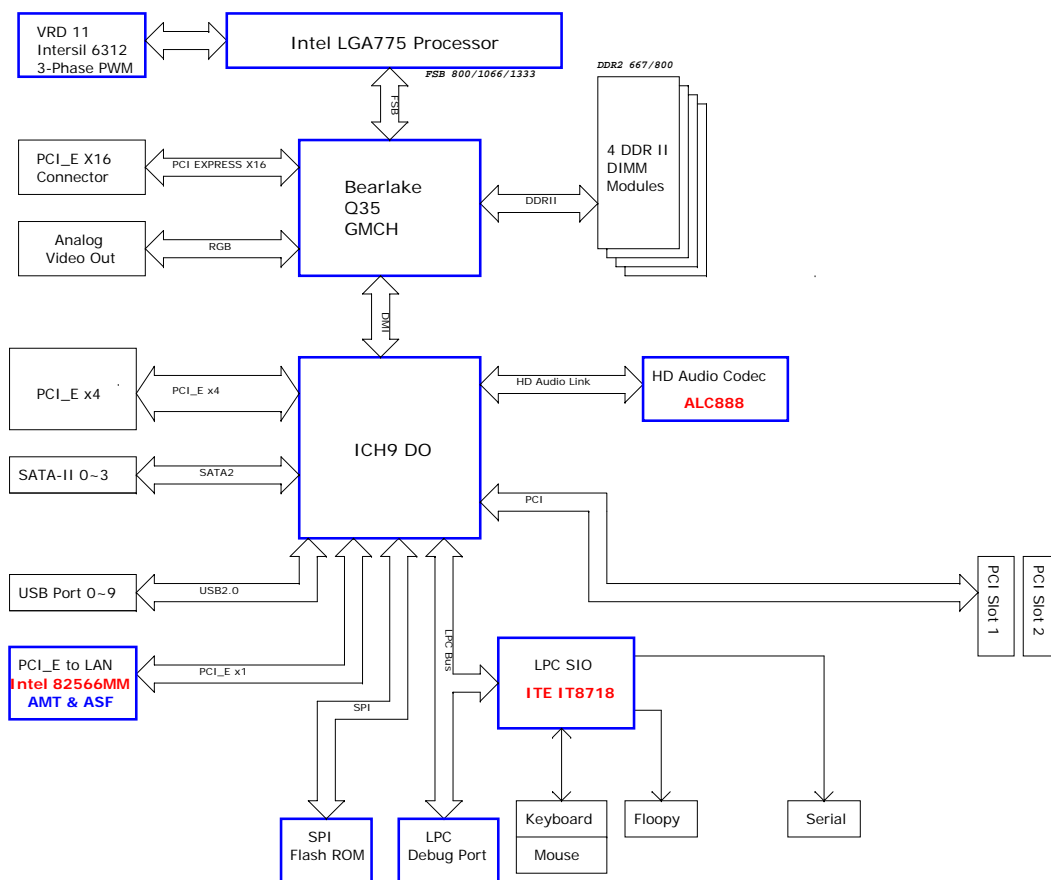
Expansion Slots:

PCI EXPRESS X16 SLOT *1
 PCI EXPRESS X1 SLOT * 2
 PCI SLOT * 1

PWM: VRD11 Intersil 6312 3Phase

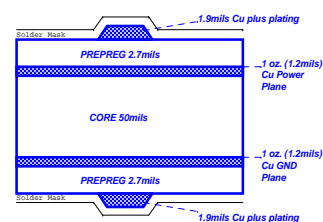
MICRO-START INT'L CO.,LTD.			
File Cover Sheet			
Size	Document Number	Rev	
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Block Diagram



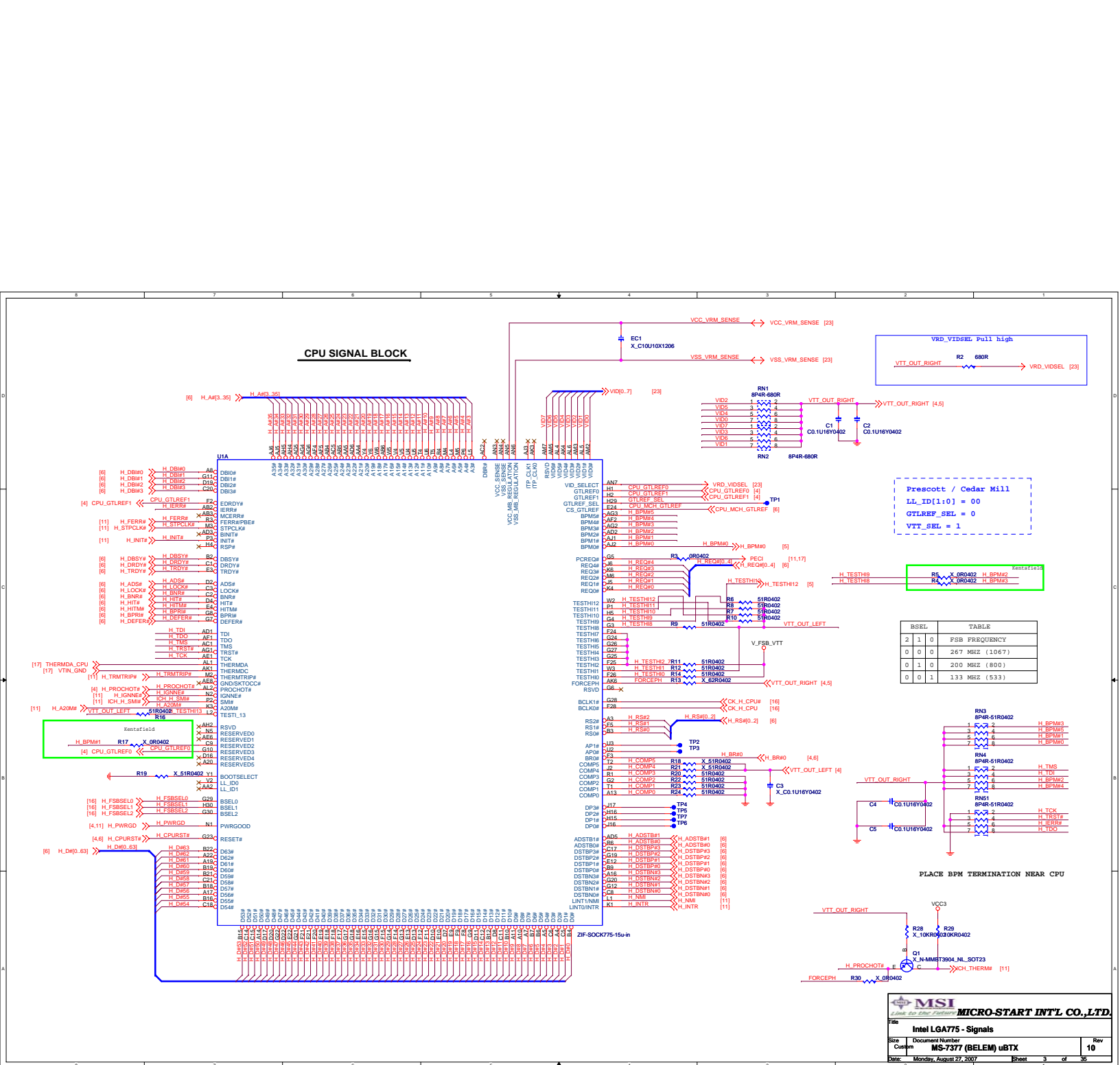
Board Stack-up

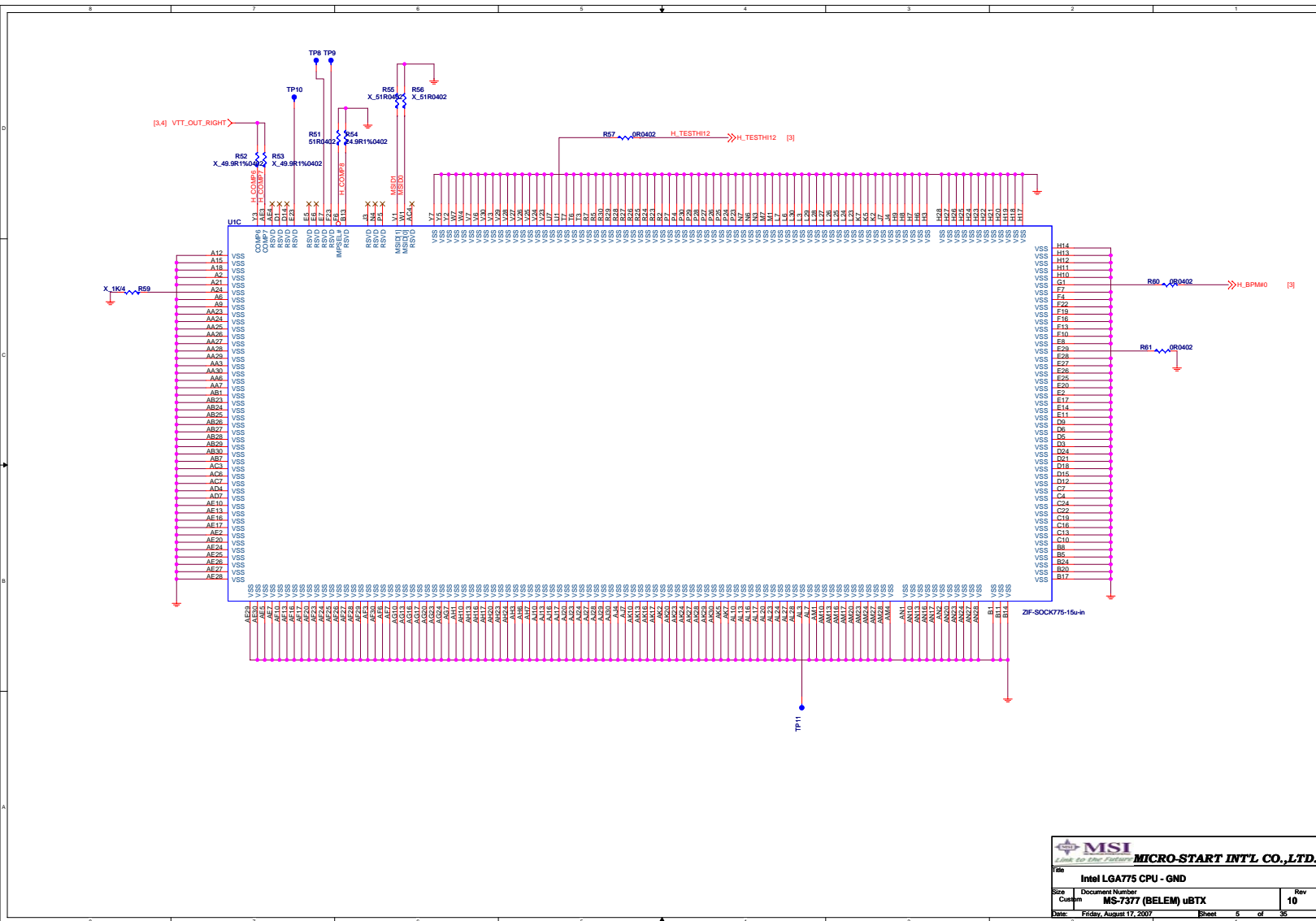
(1080 Prepreg Considerations)

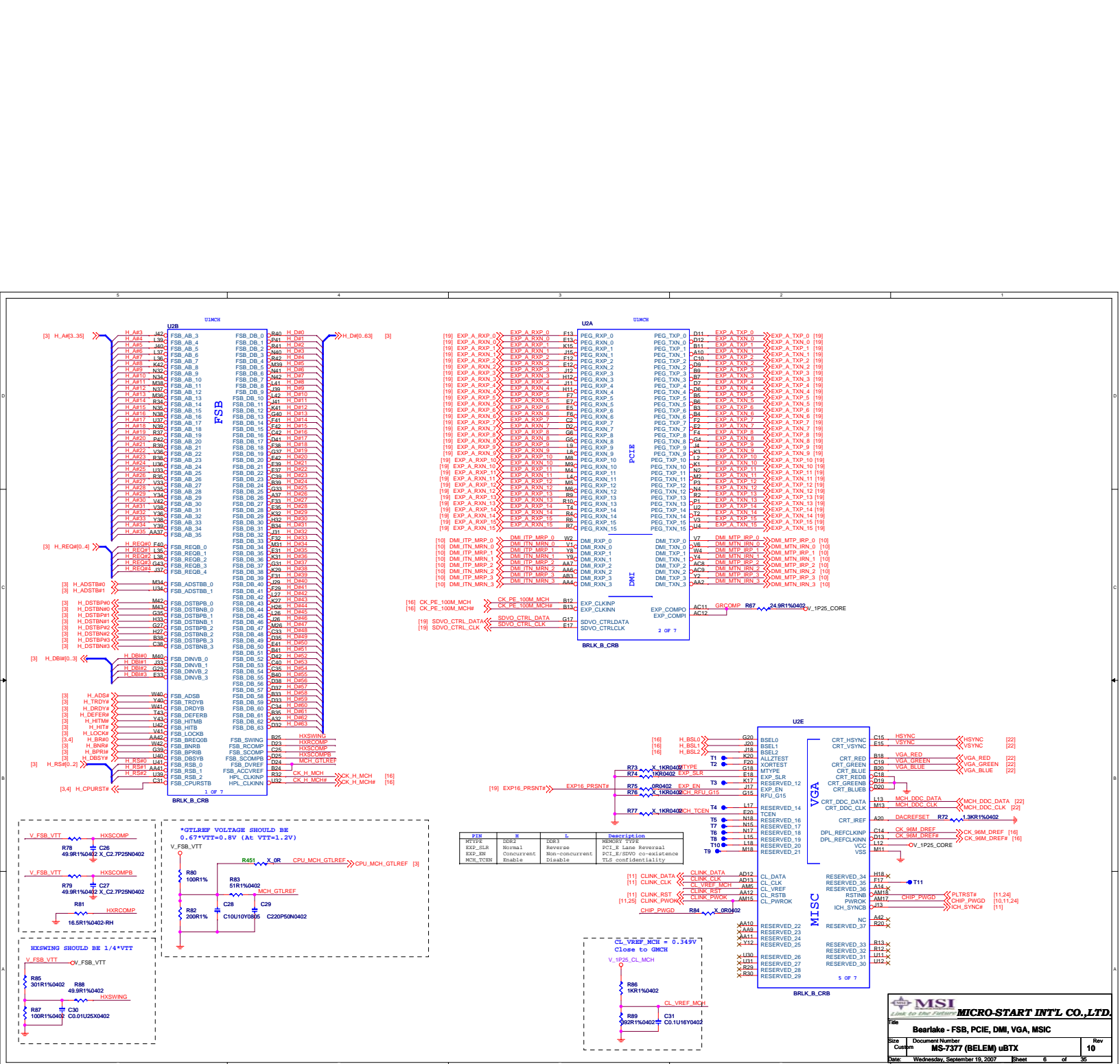


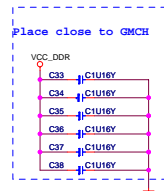
Single End 50ohm Top/Bottom : 4mils
 USB2.0 - 90ohm : 15/7.5/4.5/7.5/15
 SATA - 95ohm : 15/8/4/8/15
 LAN - 100ohm : 15/10/4/10/15
 PCIe - 95ohm : 15/8/4/8/15

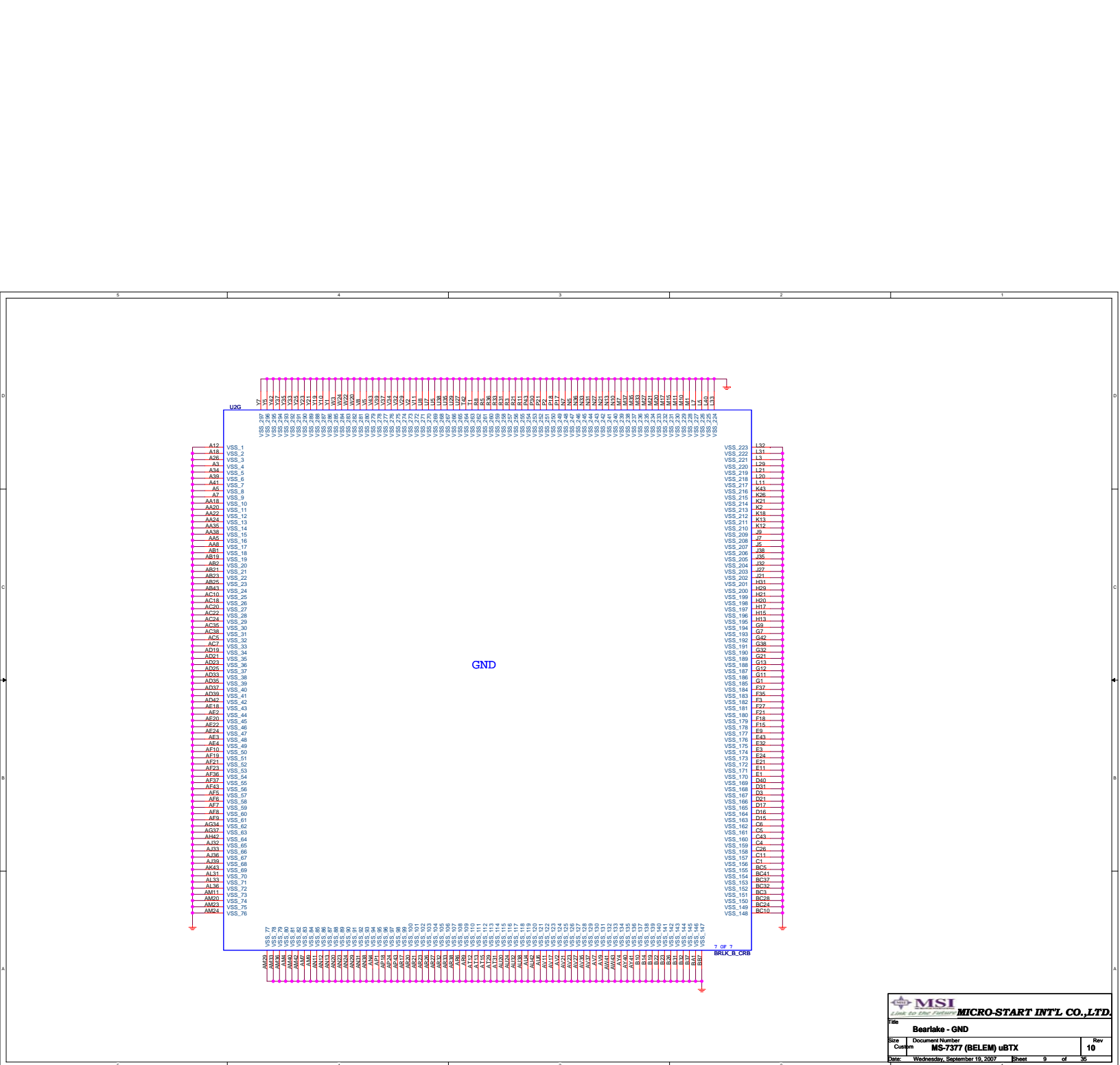
MSI MICRO-START INT'L CO., LTD.			
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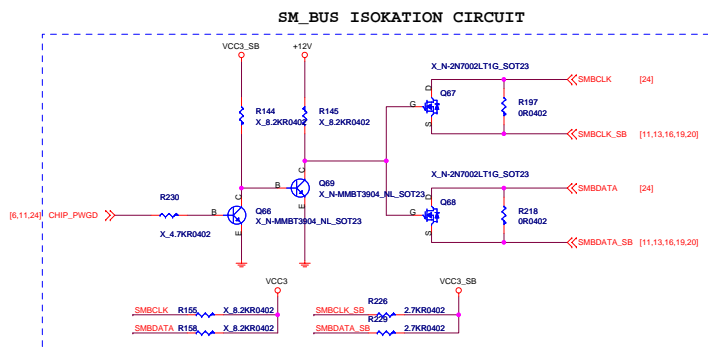
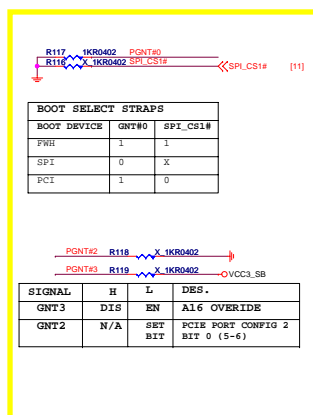
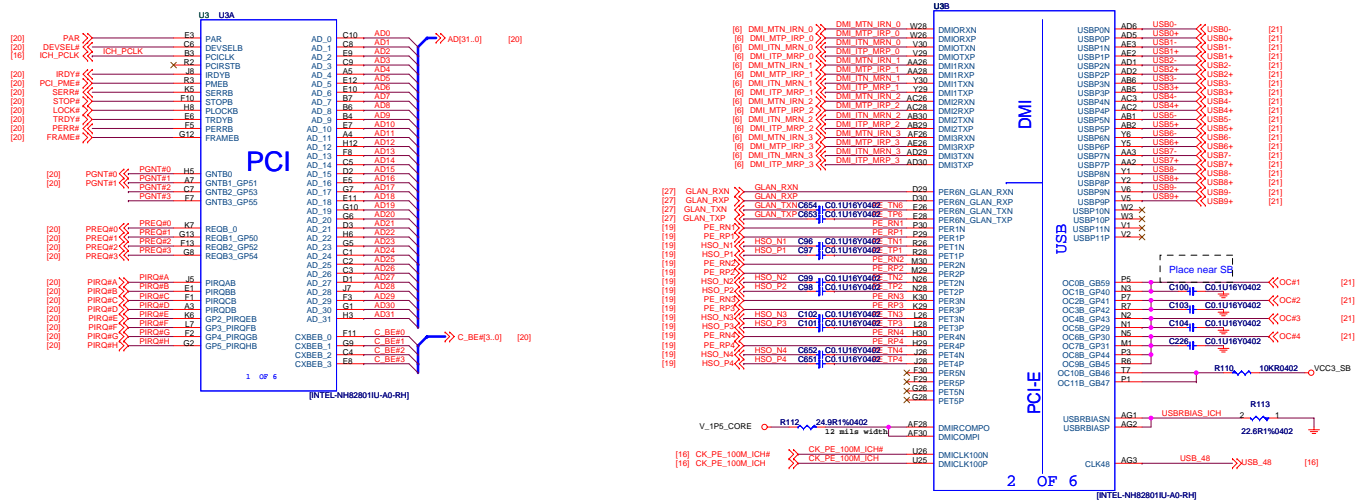




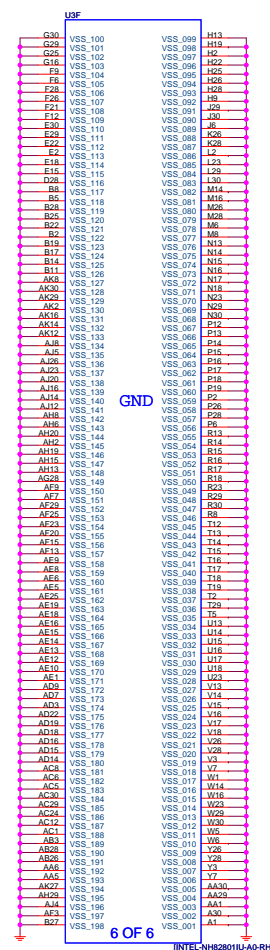
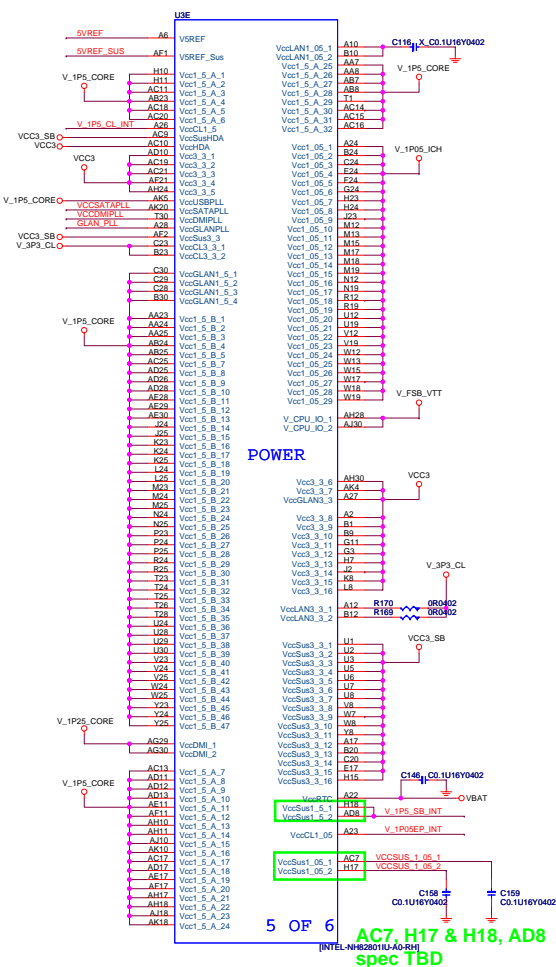
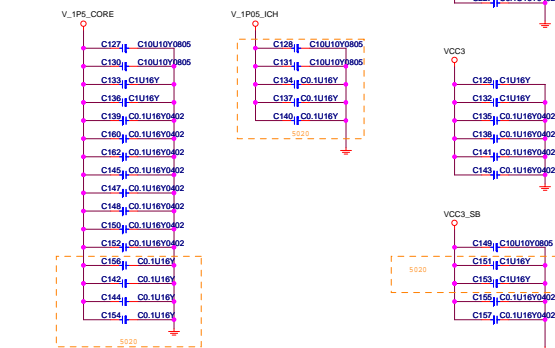


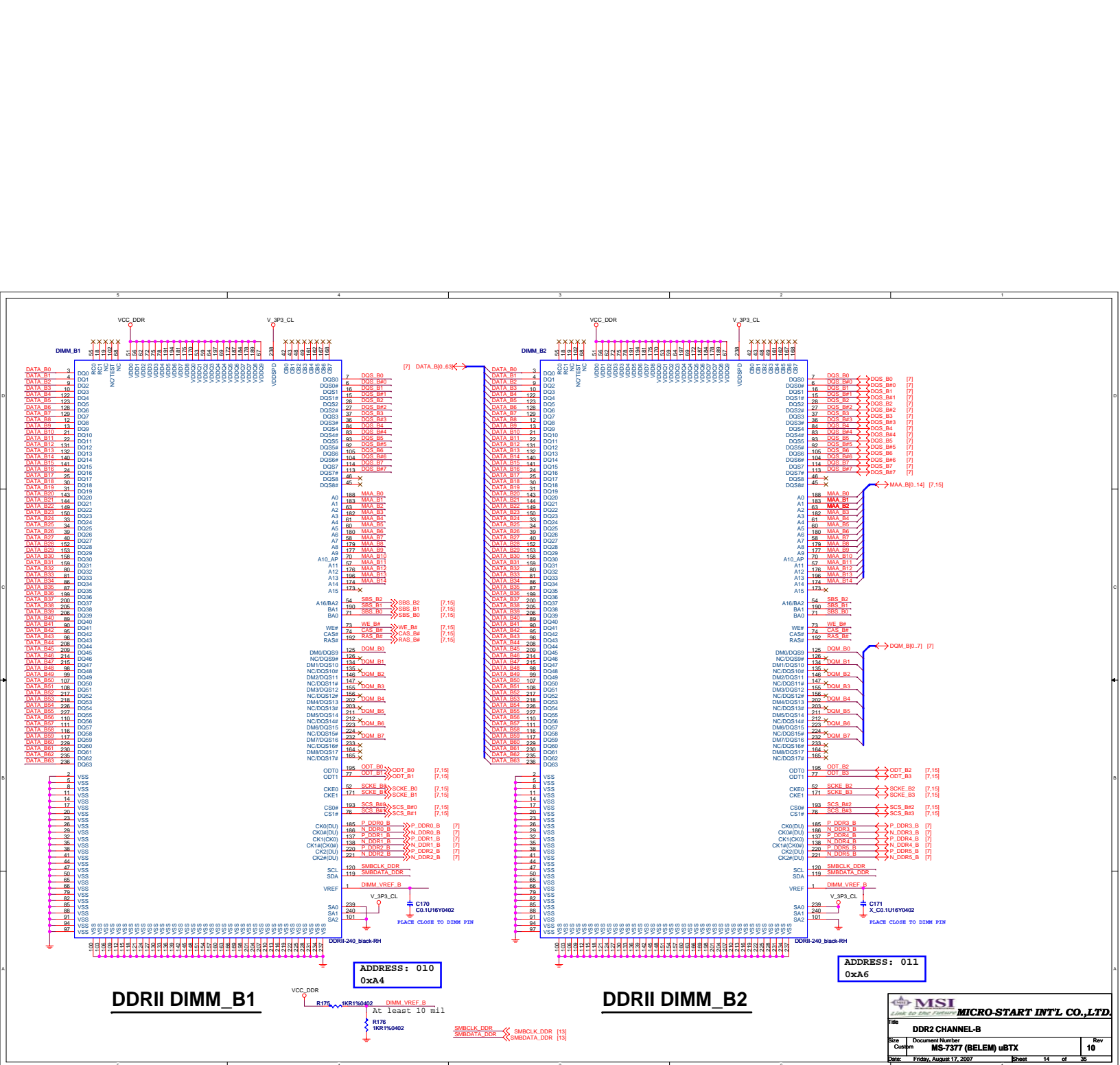






5VREF & 5VREF_SUS Sequencing Circuit



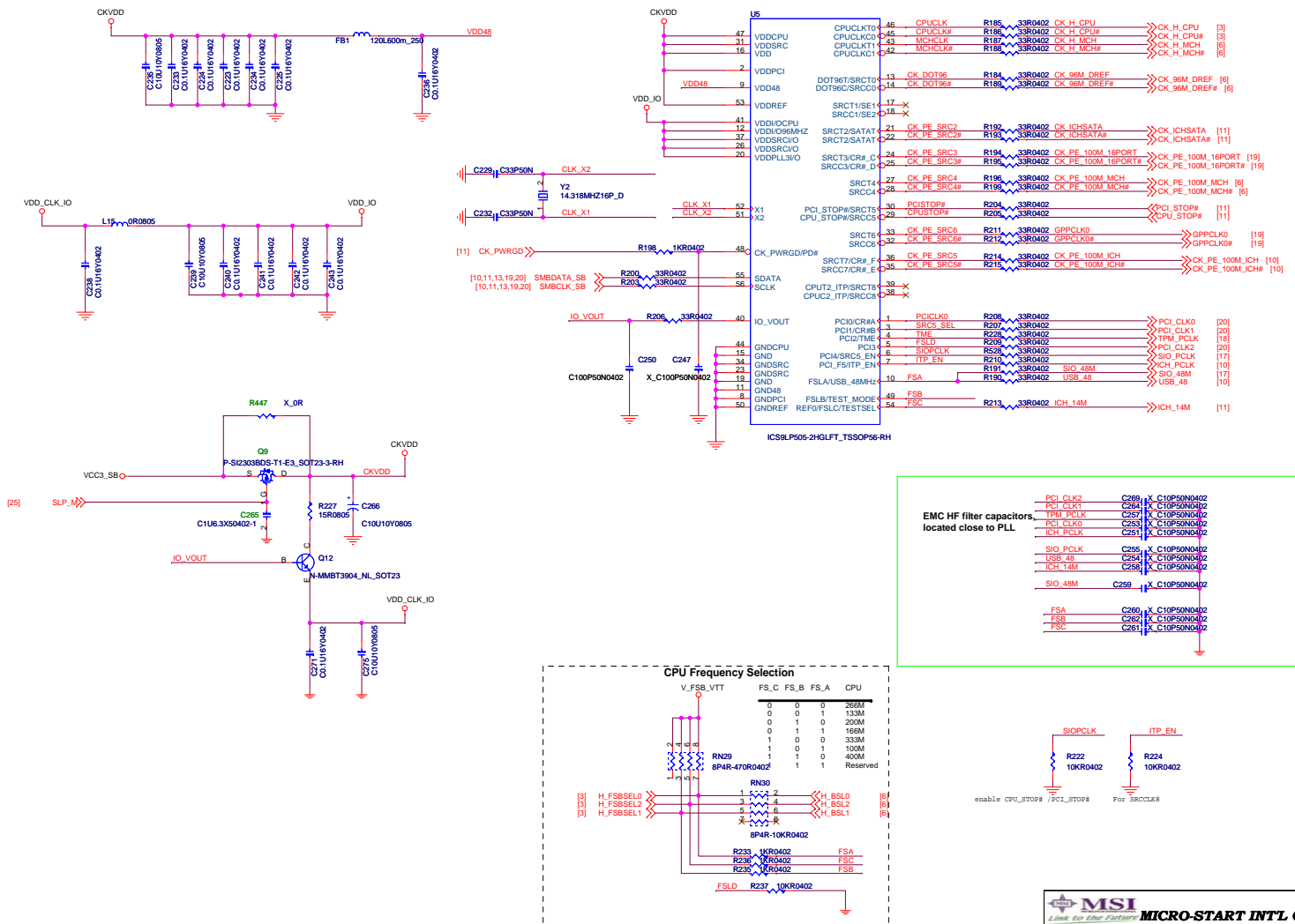


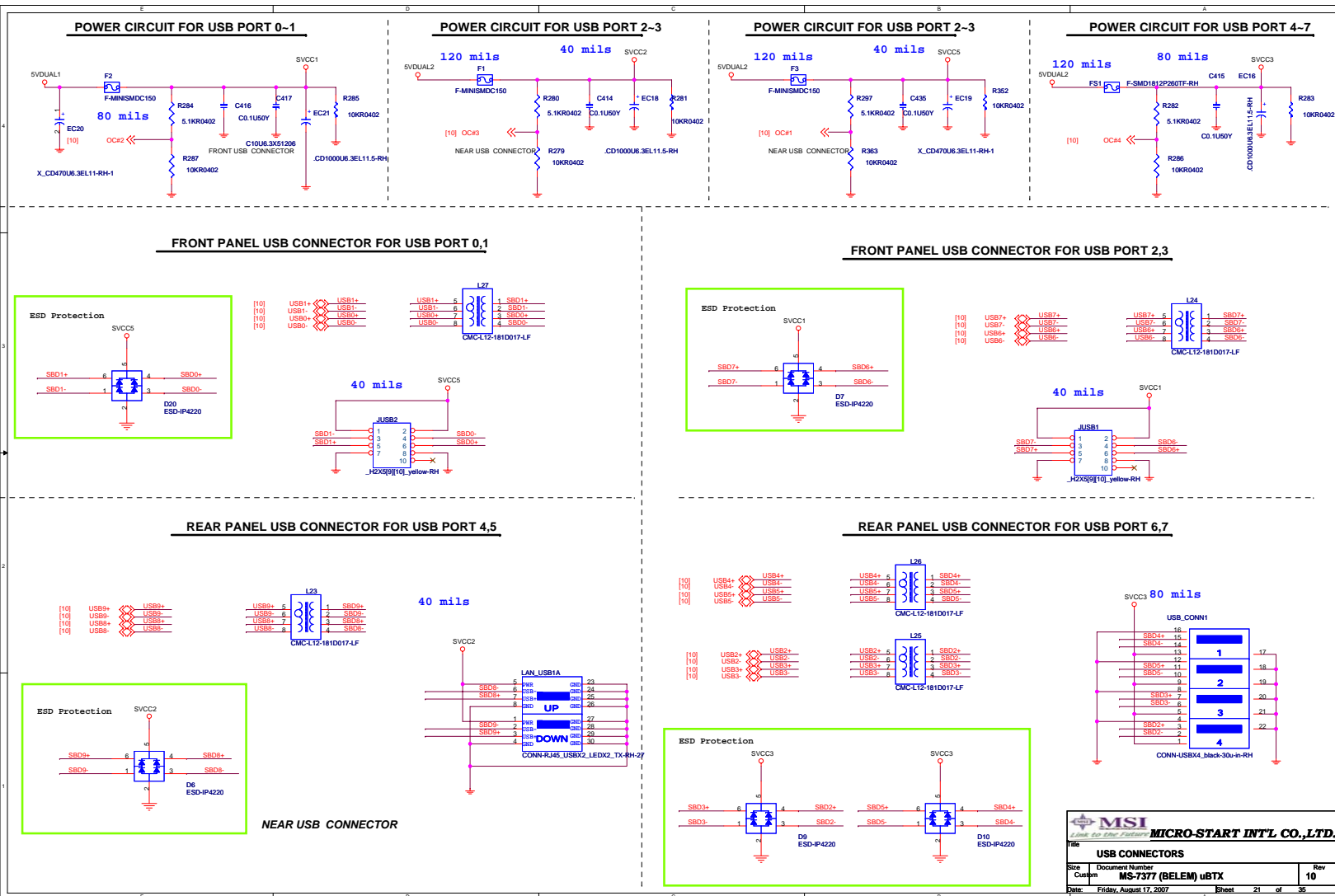
DDR II Termination

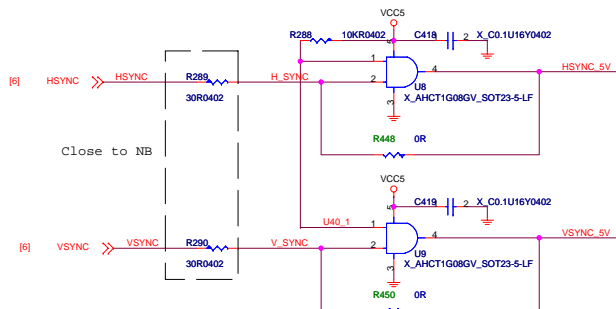


MSI Link to the Future MICRO-START INTL CO.,LTD.		
DDR II Termination		
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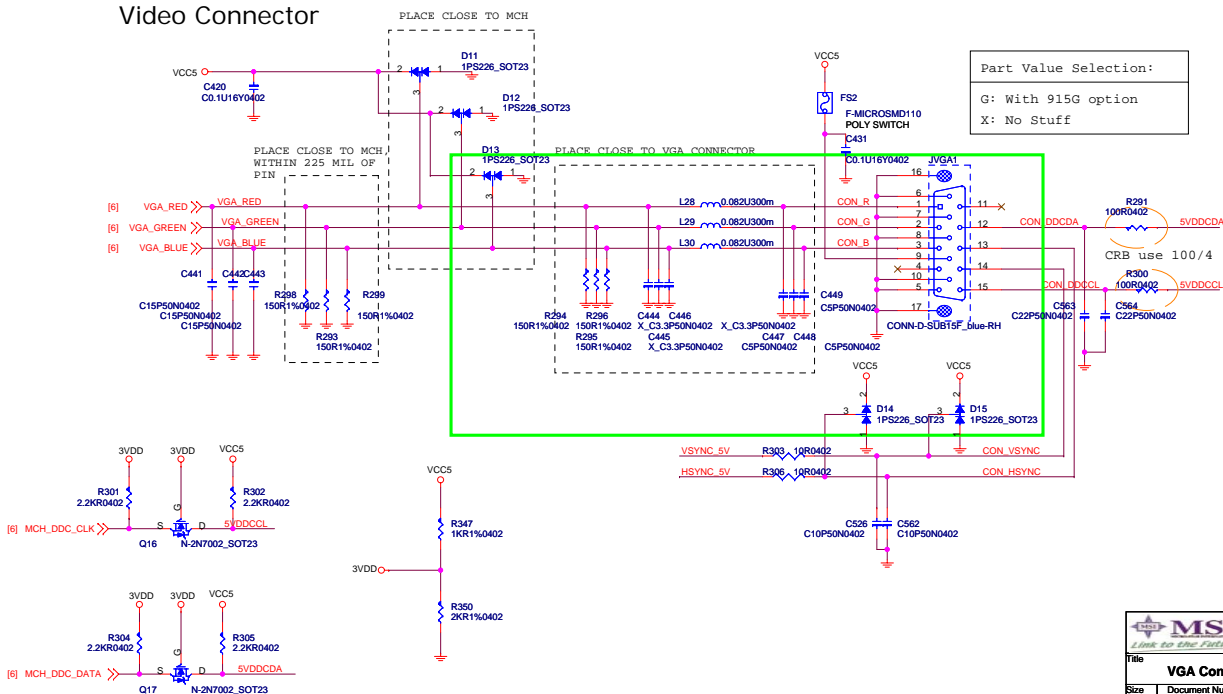
Clock Generator -ICS9LP505-2HGLFT





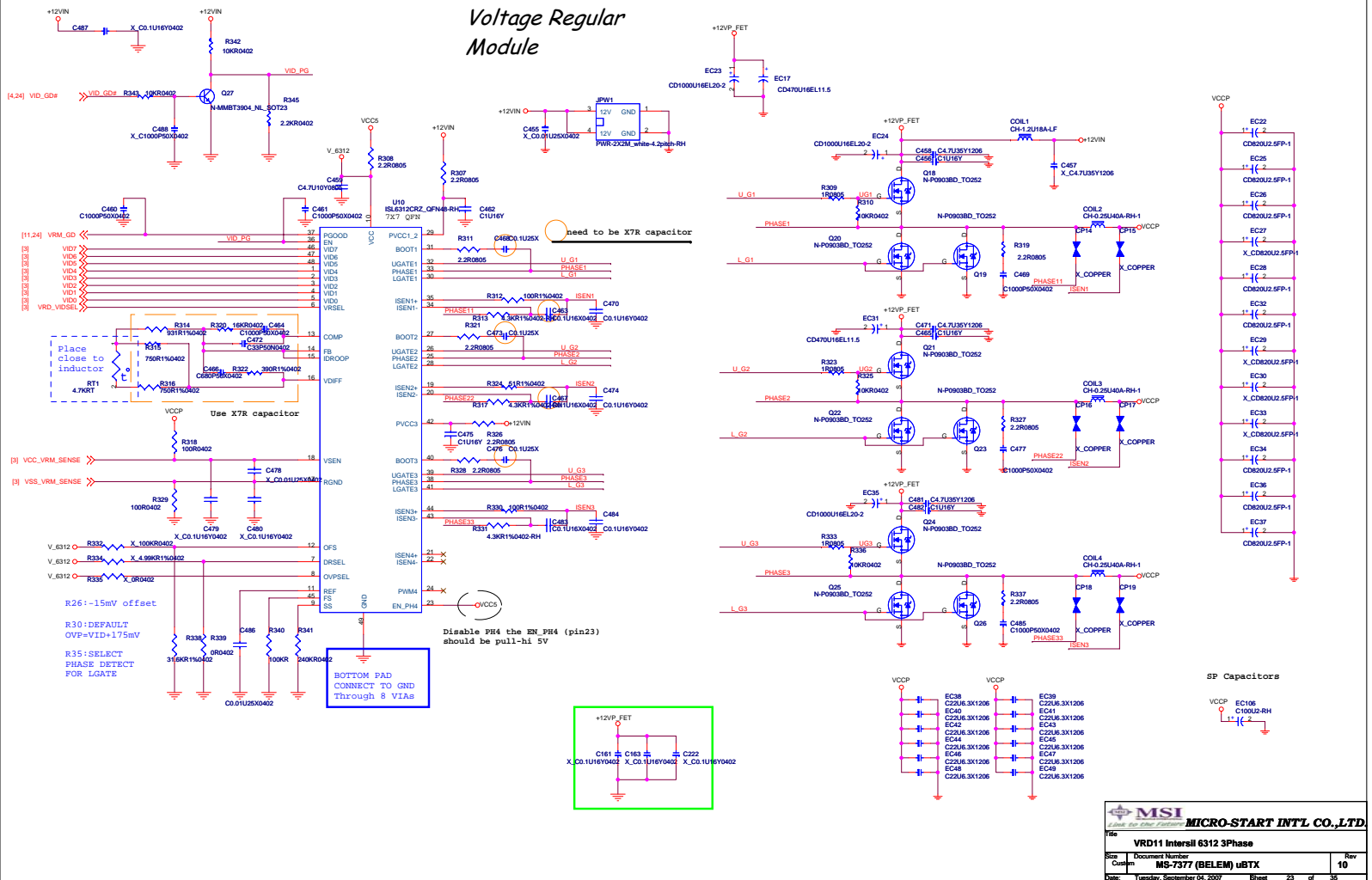


Video Connector

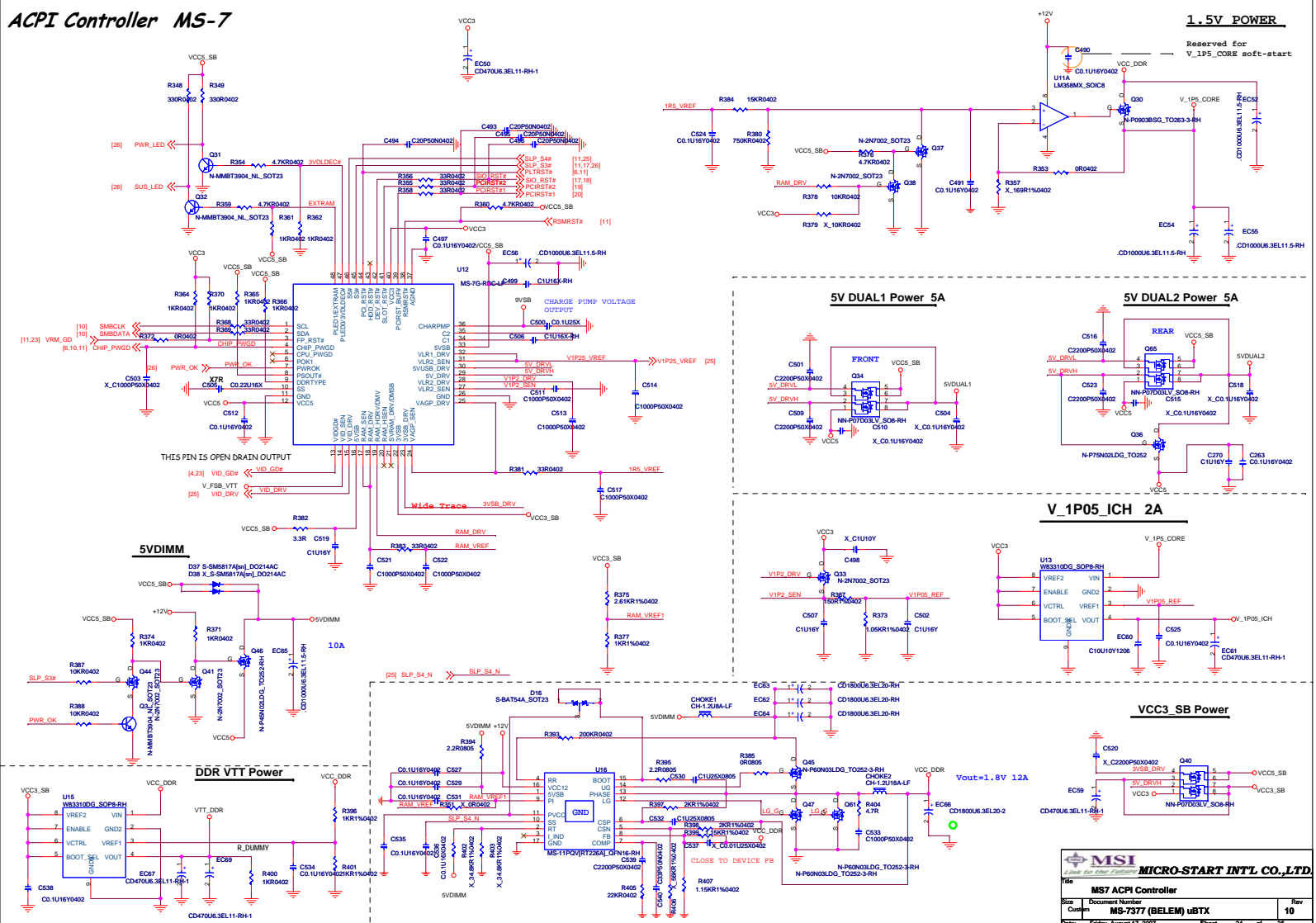


MICRO-START INT'L CO.,LTD.			
Title			
VGA Conn			
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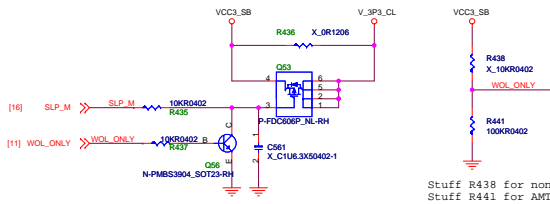
Voltage Regular Module



ACPI Controller MS-7

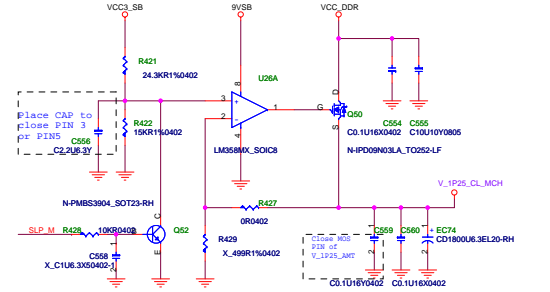


V_3P3_CL POWER 711mA

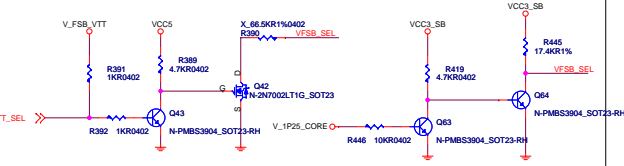


Stuff R438 for non AMT
Stuff R441 for AMT

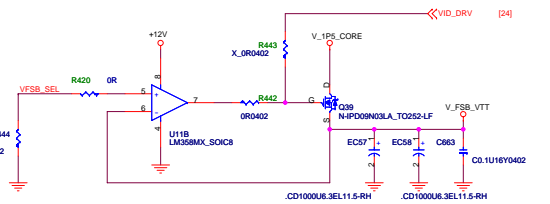
V_1P25_CL POWER 3.8A



FSB VOLTAGE SELECT CIRCUIT

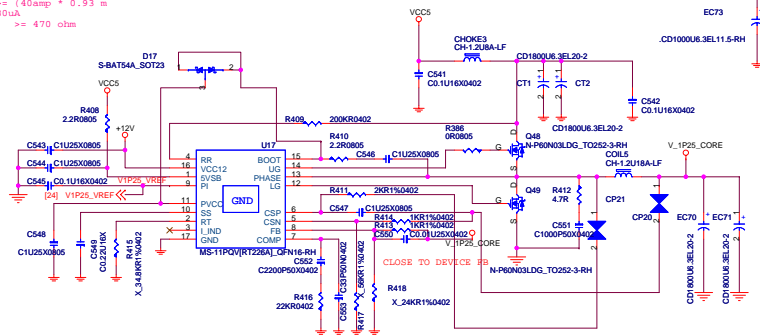


CPU FSB VTT POWER 5.8A

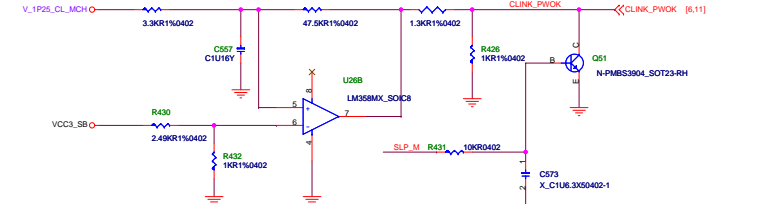


$L/DCR=R \cdot C$
 $R_{csp} \geq (0.25uV/0.93m \text{ ohm})/1uF$
 $\geq 478 \text{ ohm}$
 $I_{ocp} = DCR_{max} = I_x \cdot R_{csp}$
 $R_{csp} \geq (40amp \cdot 0.93 \text{ m ohm})/80uA$
 $\geq 470 \text{ ohm}$

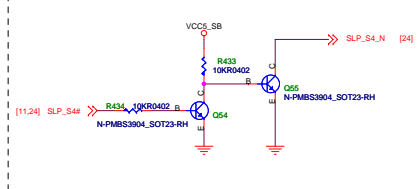
GMCH 1.25V POWER (21.3A)



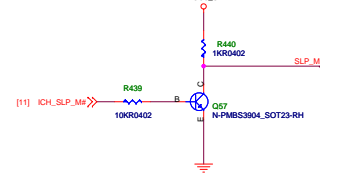
CL PWROK CIRCUIT



VCC_DDR VOLTAGE DISABLE CIRCUIT



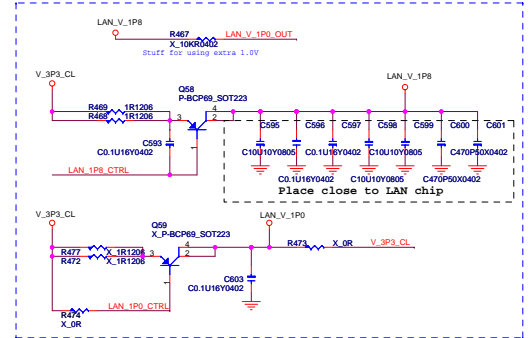
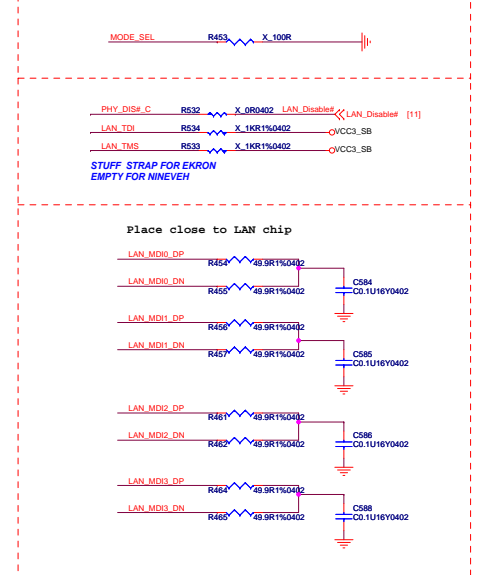
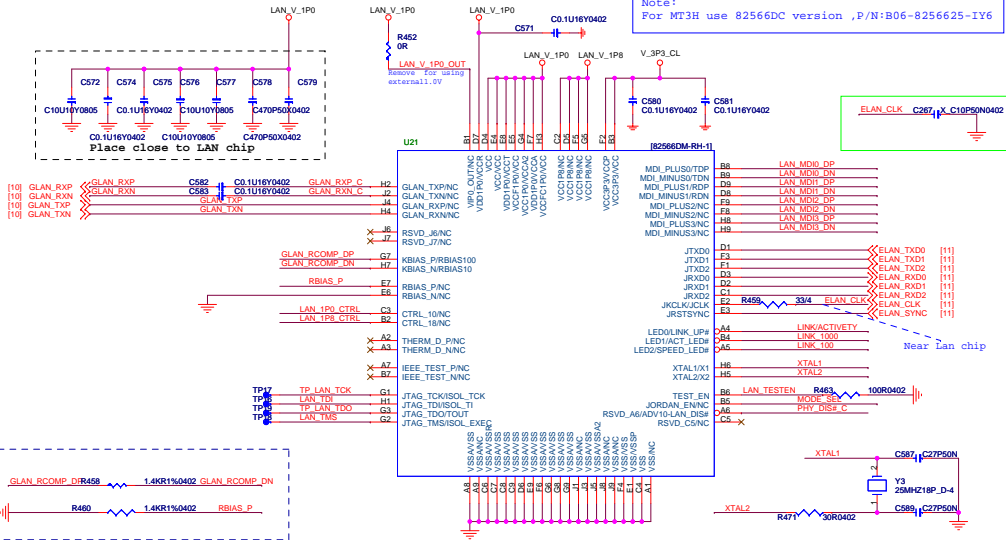
SLP_M# CONTROL CIRCUIT







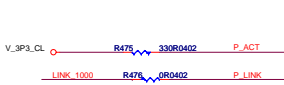
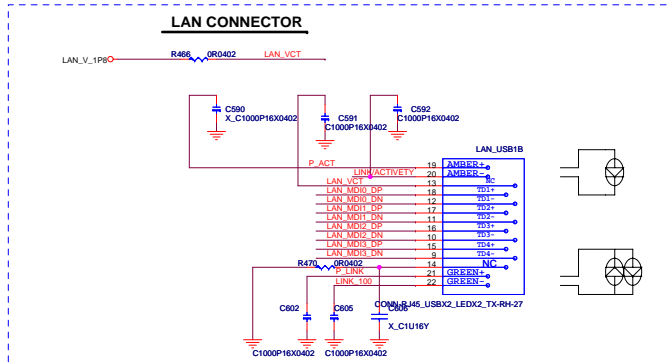
VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

MICRO-START INTL CO.,LTD.		
File	V_1P25_CORE & AMT	
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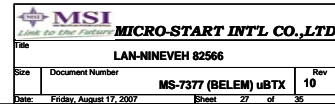
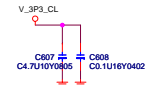
LAN - NINEVEH

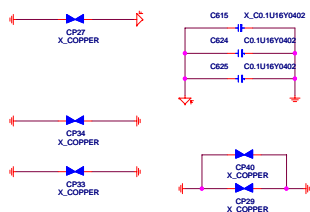



Giga-Lan		10/100-Lan	
N58-22F0081-S42		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	None	10	None
10	Green		
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	 Green	22	 Green



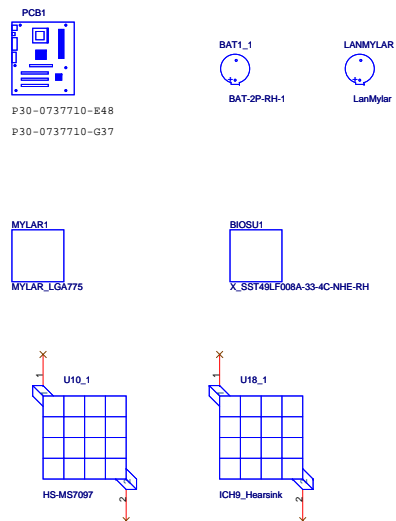
Power consumption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD



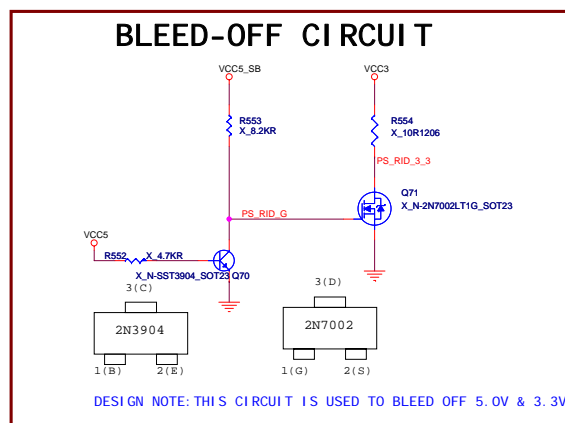
[illegible][illegible]

 MSI <i>A Look to the Future</i>				MICRO-START INT'L CO.,LTD			
Title HD Audio ALC888							
Size Custom		Document Number MS-7377 (BELEM) uBTX				Rev 10	
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MANUAL PART



Near ATX POWER Connector



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS-7377	BASELINE	cfg-7000-0A	

MSI <i>Link to the Future</i> MICRO-START INTL CO.,LTD.		
Title BLOCK DIAGRAM		
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GPIO	Alt Func	Pin	I/O/NC	Power	PU	Tol	Default	Signal Name or condition
GPIO[0]	ATADET0	N7	I/O	Vcc3	Y	3.3	INPUT	ATADET0
GPIO[1]	PULL HIGH	AK21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[2]	PIRQ#E	K6	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[3]	PIRQ#F	L7	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[4]	PIRQ#G	F2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[5]	PIRQ#H	G2	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 8.2K
GPIO[6]	PULL HIGH	AH22	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[7]	PULL HIGH	AK23	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[8]	ICH_GP8_PU	A20	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[9]	NC	A18	NC	Vcc3	N	3.3	WOL_EN	NC
GPIO[10]	ICH_GP10_PU	C17	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[11]	SMB_ALERT#	C16	I/O	Vcc3SB	Y	3.3	SMB_ALERT#	PULL HIGH 10K
GPIO[12]	NC	A8	NC	Vcc3SB	N	3.3	OUTPUT	NC
GPIO[13]	SIO_PME#	A19	I/O	Vcc3SB	Y	3.3	INPUT	SIO_PME#
GPIO[14]	ICH_GP14_PU	A9	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[15]	NC	C15	NC	Vcc3SB	Y	3.3	STP_PCI#	NC
GPIO[16]	NC	M2	NC	Vcc3	Y	3.3	OUTPUT	NC
GPIO[17]	PULL HIGH	AH21	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[18]	NC	K1	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[19]	SATA1GP_PU	AE20	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[20]	NC	AF5	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[21]	SATA0GP_PU	AK25	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[22]	ICH_SGP22_PU	AJ24	I/O	Vcc3	Y	3.3	INPUT	PULL HIGH 10K
GPIO[23]	LDRQ_1#	J3	I/O	Vcc3	Y	3.3	LDRQ_1#	PULL HIGH 10K
GPIO[24]	NC	A14	NC	Vcc3SB	N	3.3	OUTPUT	NC
GPIO[25]	NC	B18	NC	Vcc3SB	N	3.3	STP_CPU#	NC
GPIO[26]	NC	C11	NC	Vcc3SB	N	3.3	S4_STATE#	NC
GPIO[27]	NC	A11	NC	Vcc3SB	N	3.3	QRT_STATE0	NC
GPIO[28]	NC	G18	NC	Vcc3SB	N	3.3	QRT_STATE1	NC
GPIO[29]	OC#2	N1	I/O	Vcc3SB	Y	3.3	OC#2	OC#2
GPIO[30]	OC#3	N5	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[31]	OC#3	M1	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[32]	SPI_WP#	K2	I/O	Vcc3	N	3.3	OUTPUT	SPI_WP#
GPIO[33]	SPI_HOLD_GPO#	AF6	I/O	Vcc3	N	3.3	OUTPUT	SPI_HOLD_GPO#
GPIO[34]	LAN_Disable#	AH5	I/O	Vcc3	N	3.3	OUTPUT	LAN_Disable#
GPIO[35]	NC	L1	NC	Vcc3	N	3.3	OUTPUT	NC
GPIO[36]	SATA2GP_PU	AE21	I/O	Vcc3	Y	3.3	INPUT	SATA2GP_PU
GPIO[37]	SATA3GP_PU	AE22	I/O	Vcc3	Y	3.3	INPUT	SATA3GP_PU
GPIO[38]	ICH_SGP38_PU	AK24	I/O	Vcc3	Y	3.3	INPUT	ICH_SGP38_PU
GPIO[39]	ICH_SGP39_PD	AH23	I/O	Vcc3	Y	3.3	SDATAOUT0	ICH_SGP39_PD
GPIO[40]	OC#1	N3	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[41]	OC#1	P7	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[42]	OC#1	R7	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[43]	OC#2	N2	I/O	Vcc3SB	Y	3.3	OC#2	OC#2
GPIO[44]	OC#3	P3	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[45]	OC#3	R6	I/O	Vcc3SB	Y	3.3	OC#3	OC#3
GPIO[46]	PULL HIGH	T7	I/O	Vcc3SB	Y	3.3	OC#	PULL HIGH 10K
GPIO[47]	PULL HIGH	P1	I/O	Vcc3SB	Y	3.3	OC#	PULL HIGH 10K
GPIO[48]	ICH_SGP48_PD	AD20	I/O	Vcc3	Y	3.3	SDATAOUT1	PULL HIGH 10K
GPIO[49]	DMI_STRAP	AJ25	I/O	Vcc3	N	3.3	OUTPUT	PULL LOW 2.2K
GPIO[50]	PREQ#1	G13	I/O	Vcc5	Y	5.5	PREQ#1	PULL HIGH 2.7K
GPIO[51]	NC	A7	I/O	Vcc3	N	3.3	PGNT#1	NC
GPIO[52]	PREQ#2	F13	I/O	Vcc5	Y	5.5	PREQ#2	PULL HIGH 2.7K
GPIO[53]	PGNT#2	C7	I/O	Vcc3	N	3.3	PGNT#2	STRAP PIN
GPIO[54]	PREQ#3	G8	I/O	Vcc5	Y	5.5	PREQ#3	PULL HIGH 2.7K
GPIO[55]	PGNT#3	F7	I/O	Vcc3	N	3.3	PGNT#3	STRAP PIN
GPIO[56]	ICH_GP56_PU	F16	I/O	Vcc3SB	Y	3.3	GPIO_SEL	PULL HIGH 10K
GPIO[57]	ICH_GP57_PU	C12	I/O	Vcc3SB	Y	3.3	INPUT	PULL HIGH 10K
GPIO[58]	SPI_CS1#	F23	I/O	Vcc3SB	Y	3.3	SPI_CS1#	SPI_CS1#
GPIO[59]	OC#1	P5	I/O	Vcc3SB	Y	3.3	OC#1	OC#1
GPIO[60]	LINK_ALERT#	F18	I/O	Vcc3SB	Y	3.3	LINK_ALERT#	LINK_ALERT#


FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these				
GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	pull-down
FPGI[1]	5	Main	3.3	pull-high
FPGI[2]	4	Main	3.3	pull-high
FPGI[3]	3	Main	3.3	pull-high
FPGI[4]	30	Main	3.3	pull-down

PCI Config.				
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0

SIO 83627DHG				
PIN NAME	PIN#	USAGE	Input/Output	NOTES
MB_ID0	128	MB_ID0	INPUT	M/B Revision ID
MB_ID1	127	MB_ID1	INPUT	M/B Revision ID
MB_ID2	126	MB_ID2	INPUT	M/B Revision ID
MB_ID3	125	MB_ID3	INPUT	M/B Revision ID

DDRII DIMM Config.		
DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A1/MCLK_A#3 MCLK_A2/MCLK_A#4 MCLK_A2/MCLK_A#5
DIMM 3	A4H	MCLK_B0/MCLK_B#0 MCLK_B2/MCLK_B#1 MCLK_B1/MCLK_B#2
DIMM 4	A6H	MCLK_B0/MCLK_B#3 MCLK_B1/MCLK_B#4 MCLK_B2/MCLK_B#5

JUMPER SETTING		
JBAT1	(1-2) NORMAL	(2-3) CLEAR

**MICRO-START INT'L CO.,LTD**

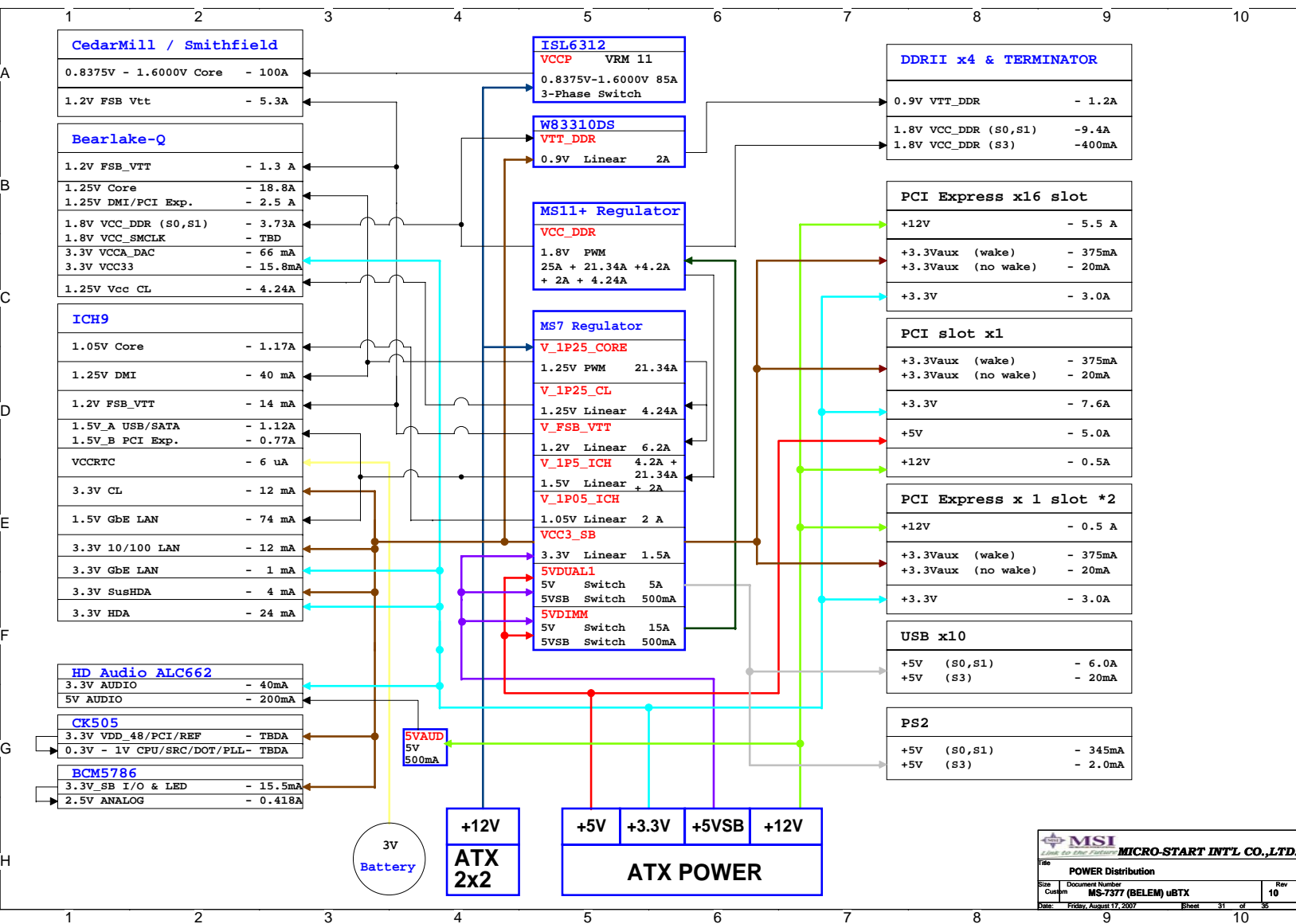
GPIO & Jumper setting

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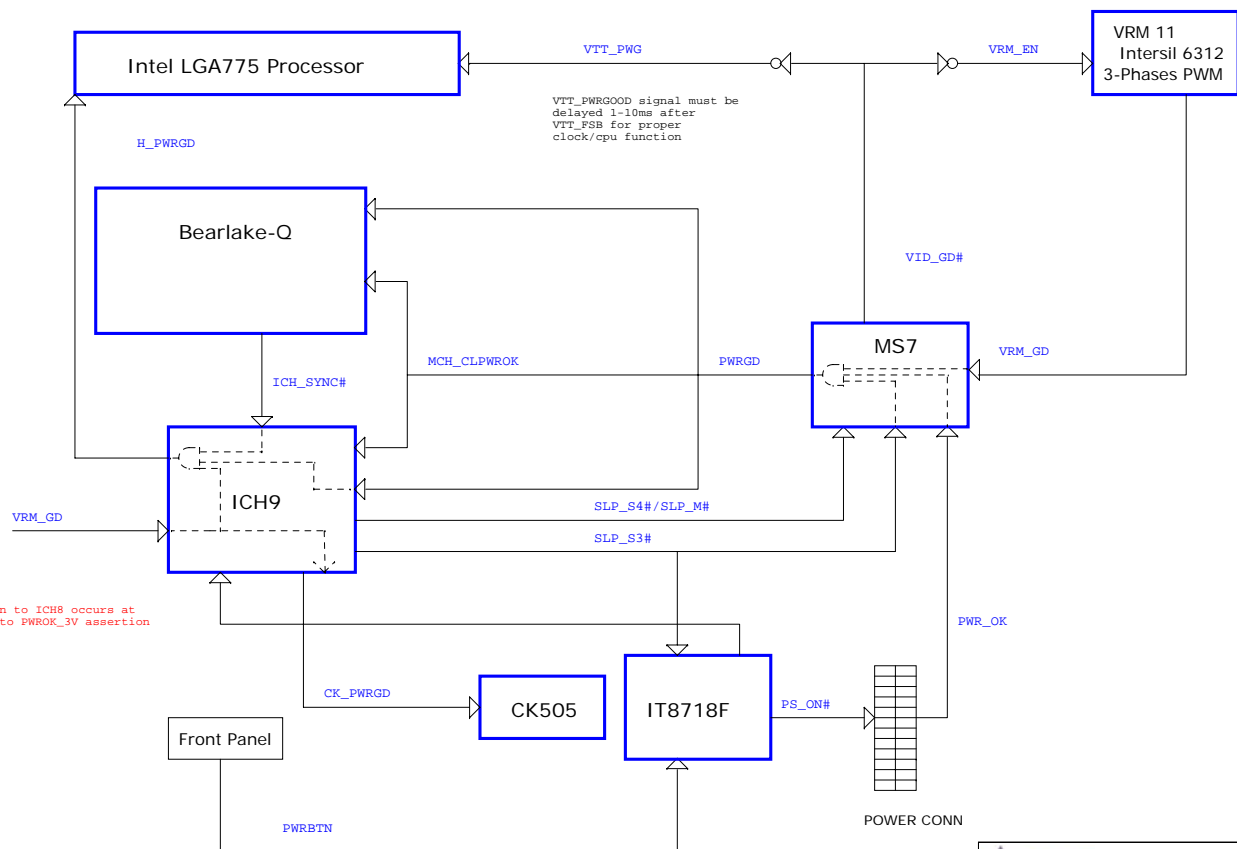
Rev 10


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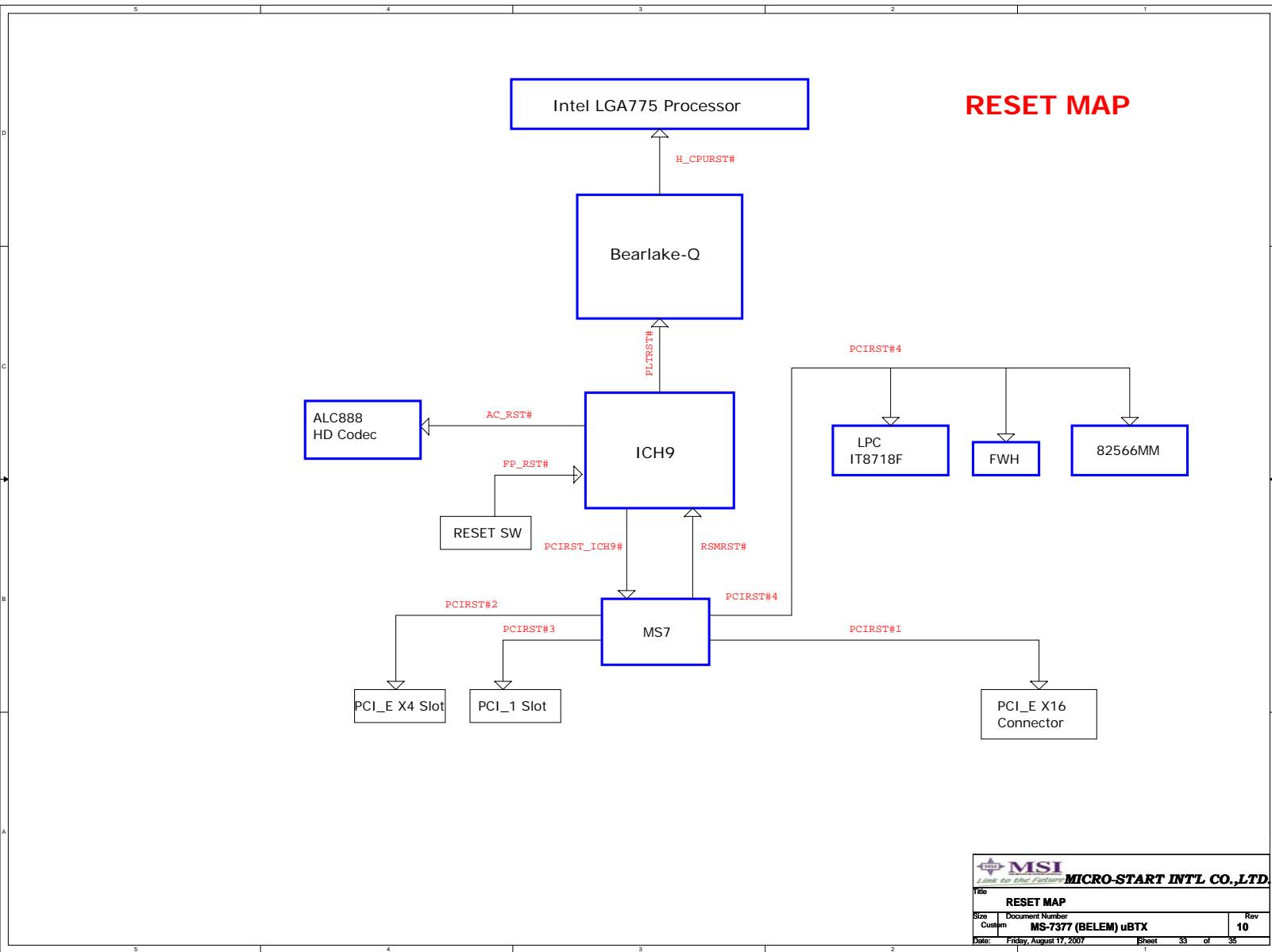
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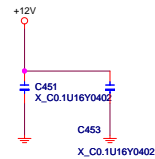
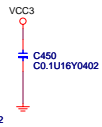
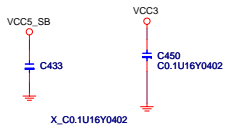
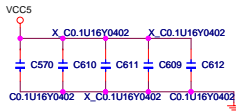
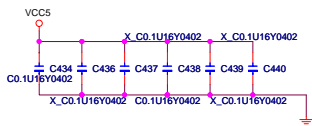
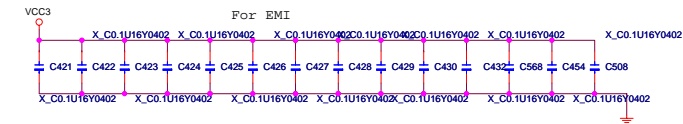
PWROK MAP



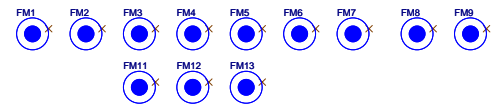
 MICRO-START INTL CO., LTD.	
PWROK MAP	
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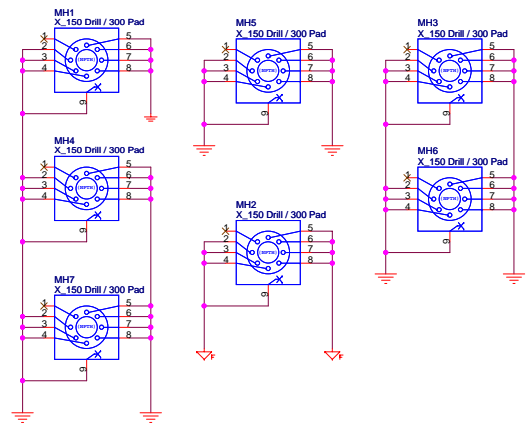
For EMI




Optical Fiducial Marks



Mounting Holes



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Version 0B

2007/06/18
1.page 4. R31 & R38 change to 1150hm
2.page 16. remove R447 , Add Q9
3.page 17. U6 pin9 & pin10(CPU_FAN) swap.
4.page 17. SOUTB R245 change to pull high.
5.page 18. Add R531 , remove R544.
6.page 22.R347 to 1KOhm, R350 to 2KOhm
7.page 22. C526 & C562 from 15P change to 10P.
8.page 22. R303 & R306 from 30 Ohm change to 10 Ohm

2007/06/20
1.page 23. EC31 from 1000uP change to 470u
2.page 23. Add EC17(470u) & EC106(SP Cap)
3.page 18. SATA connector color :SATA1 blue,SATA2 block,SATA3 orange,SATA4 block

2007/06/20
1.page 23. Q18 Q21 Q24 change to N-NTD4809NT4G_DPAK3-RH
2.page 23. Q19 Q20 Q22 Q23 Q25 Q26 change to N-P75N02LDG_TO252
3.VRM. R314 to 1KR, R315&316 to 750R,R320 to 16KR,C466 to 680pF,R322 to 390R

2007/06/20
1.DDR power . C539 to 2200pF, EC66 to 1800uF
2.NB power.C552 to 2200pF, EC70 & 71 to 1800uF, CT1 & CT2 to 1500uF


Version 10

2007/08/10
1.Change INTRUDER# from Super I/O to ICH9(pin G21). P.11
2.U27 Pin3 add 1N5817. P28
3.U27 Pin2 remover 1N5817. P28
4.R513 from 324 ohm to 300 ohm. P28
5.Add Lan Chipset Mylar Tab. P.30
6.Remove R164 for GPIO33 function. P11
7.Remove R240 for SIO_PME# function. P17

2007/08/12 CPU side power change List (VRM)
1.Remove EC1. P3
2.change R324 from 100 ohm to 51 ohm. P23
3.change EC38 EC39 EC40 EC41 EC42 EC43 EC44 EC45 EC46 EC47 EC48 EC49 from 10uF to 22uF. P23.
4.Change R313 R317 R331 from 5.49Kohm to 4.3Kohm. P23.
5.change R314 from 1KOhm to 9310hm. P23.
6.change R338 from 42.2KOhm to 31.6KOhm. P23.
7.change R340 from 120KOhm to 100KOhm. P23.
8.Add EC32. P23.

Version 11

2007/09/20
1.Add R132 & R135 for ICH9 PCIE-X4 function. P11

 MSI <i>Link to the Future</i> MICRO-START INTL CO.,LTD.		
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