MANUFACTURING DESCRIPTION	
Module Manufacturer:	G.Skill
Module Part Number:	F4-4133C19-8GTZA
Module Series:	Trident Z
DRAM Manufacturer:	Samsung
DRAM Components:	K4A8G085WB-BCPB
DRAM Die Revision / Process Node:	B / 20 nm
Module Manufacturing Date:	Undefined
Module Manufacturing Location:	Taipei, Taiwan
Module Serial Number:	00000000h
Module PCB Revision:	00h

PHYSICAL & LOGICAL ATTRIBUTES	
Fundamental Memory Class:	DDR4 SDRAM
Module Speed Grade:	DDR4-2133
Base Module Type:	UDIMM (133,35 mm)
Module Capacity:	8192 MB
Reference Raw Card:	A1 (8 layers)
Initial Raw Card Designer:	SK hynix
Module Nominal Height:	31 < H <= 32 mm
Module Thickness Maximum, Front:	1 < T <= 2 mm
Module Thickness Maximum, Back:	1 < T <= 2 mm
Number of DIMM Ranks:	1
Address Mapping from Edge Connector to DRAM:	Standard
DRAM Device Package:	Standard Monolithic
DRAM Device Package Type:	78-ball FBGA
DRAM Device Die Count:	Single die
Signal Loading:	Not specified
Number of Column Addresses:	10 bits
Number of Row Addresses:	16 bits
Number of Bank Addresses:	2 bits (4 banks)
Bank Group Addressing:	2 bits (4 groups)
DRAM Device Width:	8 bits
Programmed DRAM Density:	8 Gb
Calculated DRAM Density:	8 Gb
Number of DRAM components:	8
DRAM Page Size:	1 KB
Primary Memory Bus Width:	64 bits
Memory Bus Width Extension:	0 bits
DRAM Post Package Repair:	Supported
Soft Post Package Repair:	Supported

DRAM TIMING PARAMETERS	
Fine Timebase:	0,001 ns
Medium Timebase:	0,125 ns
CAS Latencies Supported:	10T, 11T, 12T, 13T, 14T, 15T, 16T
Minimum Clock Cycle Time (tCK min):	0,938 ns (1066,10 MHz)
Maximum Clock Cycle Time (tCK max):	1,600 ns (625,00 MHz)
CAS# Latency Time (tAA min):	13,750 ns
RAS# to CAS# Delay Time (tRCD min):	13,750 ns
Row Precharge Delay Time (tRP min):	13,750 ns
Active to Precharge Delay Time (tRAS min):	33,000 ns
Act to Act/Refresh Delay Time (tRC min):	46,750 ns
Normal Refresh Recovery Delay Time (tRFC1 min):	350,000 ns
2x mode Refresh Recovery Delay Time (tRFC2 min):	260,000 ns
4x mode Refresh Recovery Delay Time (tRFC4 min):	160,000 ns
Short Row Active to Row Active Delay (tRRD_S min):	3,700 ns
Long Row Active to Row Active Delay (tRRD_L min):	5,300 ns
Write Recovery Time (tWR min):	15,000 ns
Short Write to Read Command Delay (tWTR_S min):	2,500 ns
Long Write to Read Command Delay (tWTR_L min):	7,500 ns
Long CAS to CAS Delay Time (tCCD_L min):	5,625 ns
Four Active Windows Delay (tFAW min):	21,000 ns
Maximum Active Window (tMAW):	8192*tREFI
Maximum Activate Count (MAC):	Unlimited MAC
DRAM VDD 1,20 V operable/endurant:	Yes/Yes

THERMAL PARAMETERS	
Module Thermal Sensor:	Not Incorporated

SPD PROTOCOL	
SPD Revision:	1.1
SPD Bytes Total:	512
SPD Bytes Used:	384

SPD Checksum (Bytes 00h-7Dh):	242Dh (OK)
SPD Checksum (Bytes 80h-FDh):	A01Ch (OK)

PART NUMBER DETAILS

JEDEC DIMM Label:	8GB 1Rx8 PC4-2133-UA1-11

FREQUENCY	CAS	RCD	RP	RAS	RC	RRDS	RRDL	WR	WTRS	WTRL	FAW
1067 MHz	16	15	15	36	50	4	6	16	3	8	23
1067 MHz	15	15	15	36	50	4	6	16	3	8	23
933 MHz	14	13	13	31	44	4	5	14	3	7	20
933 MHz	13	13	13	31	44	4	5	14	3	7	20
800 MHz	12	11	11	27	38	3	5	12	2	6	17
800 MHz	11	11	11	27	38	3	5	12	2	6	17
667 MHz	10	10	10	22	32	3	4	10	2	5	14

INTEL EXTREME MEMORY PROFILES

Profiles Revision: 2.0

Profile 1 (Certified) Enables: Yes

Profile 2 (Extreme) Enables: No

Profile 1 Channel Config: 2 DIMM/channel

XMP PARAMETER	PROFILE 1	PROFILE 2
Speed Grade:	DDR4-4140	N/A
DRAM Clock Frequency:	2070 MHz	N/A
Module VDD Voltage Level:	1,35 V	N/A
Minimum DRAM Cycle Time (tCK):	0,483 ns	N/A
CAS Latencies Supported:	19T	N/A
CAS Latency Time (tAA):	9,073 ns	N/A
RAS# to CAS# Delay Time (tRCD):	10,107 ns	N/A
Row Precharge Delay Time (tRP):	10,107 ns	N/A
Active to Precharge Delay Time (tRAS):	19,750 ns	N/A
Active to Active/Refresh Delay Time (tRC):	29,804 ns	N/A
Four Activate Window Delay Time (tFAW):	24,000 ns	N/A
Short Activate to Activate Delay Time (tRRD_S):	3,500 ns	N/A
Long Activate to Activate Delay Time (tRRD_L):	5,000 ns	N/A
Normal Refresh Recovery Delay Time (tRFC1):	350,000 ns	N/A
2x mode Refresh Recovery Delay Time (tRFC2):	260,000 ns	N/A
4x mode Refresh Recovery Delay Time (tRFC4):	160,000 ns	N/A

Show delays in clock cycles